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Search History

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L3	L2 and l1	339	L3
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L17: Entry 1 of 1 File: USPT Oct 3, 2000

DOCUMENT-IDENTIFIER: US 6128757 A
TITLE: Low voltage screen for improving the fault coverage of integrated circuit production test programs

Abstract Text (1):
A method for improving the fault coverage of functional tests for integrated circuits by establishing a design-specific low voltage functional screening procedure. In the disclosed embodiment of the invention, a reduced voltage test threshold is established by comparing the results of an iterative test procedure executed on a set of known good integrated circuits and integrated circuits which have passed traditional functional test programs but manifested problems in the field. For a given device under test, the iterative procedure commences by applying a system clock and nominal power supply voltage. A set of functional test vectors is then executed on the device using automated test equipment (ATE). The results are compared with expected test results to determine if the device is a passing device under the initial test conditions. If so, the power supply voltage is decremented by a predetermined value and the test process is repeated. This iterative process continues until the device under test fails the functional test. At this point, the power supply voltage at which the device under test has failed functional testing or, alternatively, the previous power supply voltage, is stored in a database. The testing procedure is then repeated for a statistically significant group of additional known good parts/bad parts. After databases have been compiled for the good and bad parts, the results of the testing procedure are examined to determine the voltage below which substantially all the known good parts pass and above which substantially all the bad parts fail. This voltage is then utilized as the reduced voltage test threshold value for a production test program. Additional information relating to the integrity of the semiconductor process used to manufacture the devices under test may also be compiled to verify that the results of the test development procedure have not been skewed.

Brief Summary Text (11):
Following fabrication of an integrated circuit, testing is performed to insure that the integrated circuit functions as designed. Although the integrated circuit may work functionally, it may not operate at the clock frequency at which it was designed to operate. Certain testing methodologies are employed to verify that the integrated circuit works "at speed." One such method is to test all circuitry functionally at the highest frequency at which the integrated circuit is designed to operate. At speed testing of all circuitry is typically not performed, however, because it is extremely difficult to create test patterns to verify an entire integrated circuit at the higher frequencies at which today's integrated circuits operate. Further, specialized testers are also required.

Brief Summary Text (19):
In the disclosed embodiment of the invention, a reduced voltage test threshold is established by comparing the results of an iterative test procedure executed on a set of known good integrated circuits and integrated circuits which have passed traditional functional test programs but manifested problems in the field. For a given device under test, the iterative procedure commences by applying a system

clock and nominal power supply voltage to the device under test. A set of functional test vectors is then executed on the device using ATE. The results are compared with expected test results to determine if the device is a passing device under the initial test conditions. If so, the power supply voltage is decremented by a predetermined value and the test process is repeated. This iterative process continues until the device under test fails the functional test.

Detailed Description Text (6):
Next, in step 204, functional test vectors from a specialized test program are executed and applied to the inputs of the device under test 108. Results of the test program are retrieved in step 206. These results are then compared, in step 208, with data representing expected test results corresponding to the test vectors of step 204.

Detailed Description Text (9):
Following either of steps 218 or 222, and assuming that enough devices have been tested to form a statistically significant sample, the testing procedure continues to step 224 and the first and second ATE datalogs DATALOG1 and DATALOG2 are compared to ascertain the power supply voltage or range of voltages below which substantially all of the known good parts pass functional testing and above which substantially all of the "bad" parts fail functional testing. This voltage is referred to herein as the low voltage screen VDDS threshold. Next, in step 226, the low voltage screen VDDS threshold, is stored for use in a low voltage screening process of a production test program such as that described below in conjunction with FIG. 3. The test development procedure then ends in step 228.

CLAIMS:

1. A method for developing a low voltage screening process for testing integrated circuits on automated test equipment, the method comprising the steps of: providing an integrated circuit for testing;

applying a first power supply voltage to the integrated circuit;

executing test vectors of a functional test program the integrated circuit;

comparing the results of the functional test program with expected test results to determine if the integrated circuit passes the functional test; and, if so,

iteratively decrementing the first power supply voltage by a predetermined value and repeating the steps of executing test vectors and comparing the results until it is determined that the integrated circuit fails the functional test; and

storing a value representing the power supply voltage at which the integrated circuit first fails the functional test.

2. The method of claim 1, further comprising the steps of:

repeating each of the previous steps for additional integrated circuits; and

comparing the stored values to identify the lowest tested power supply voltage below which substantially all of the integrated circuits pass the functional test, the identified power supply voltage being useful for establishing a reduced voltage screening procedure for a production test program.

11. A method for testing integrated circuits on automated test equipment, the method incorporating a low voltage screening procedure, comprising the steps of:

providing an integrated circuit for testing;

applying a first power supply voltage to the integrated circuit, the first power supply voltage within the range of specified operating voltages for the integrated circuit;

executing test vectors of a production test program on the integrated circuit;

comparing the results of the production test program with expected test results to determine if the integrated circuit passes the production test program; and, if so,

reducing the first power supply voltage to a predetermined reduced voltage screening value;

executing test vectors of a screening test program on the integrated circuit; and

comparing the results of the screening test program with expected test results to determine if the integrated circuit passes the screening test program.

12. The method of claim 11, wherein the production test program and the screening test program are functional tests programs.

13. The method of claim 12, wherein the production test program and the screening test program are substantially the same.

20. The method of claim 19, wherein the screening test program is performed at a clock frequency less than the nominal operating frequency of the integrated circuit.

21. The method of claim 11, wherein the screening test program is performed at room temperature.

22. The method of claim 11, further comprising the step of marking the integrated circuit as a bad device if it fails the screening test program.

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L13: Entry 4 of 8 File: USPT Oct 3, 2000

DOCUMENT-IDENTIFIER: US 6128757 A
TITLE: Low voltage screen for improving the fault coverage of integrated circuit production test programs

Brief Summary Text (11):
Following fabrication of an integrated circuit, testing is performed to insure that the integrated circuit functions as designed. Although the integrated circuit may work functionally, it may not operate at the clock frequency at which it was designed to operate. Certain testing methodologies are employed to verify that the integrated circuit works "at speed." One such method is to test all circuitry functionally at the highest frequency at which the integrated circuit is designed to operate. At speed testing of all circuitry is typically not performed, however, because it is extremely difficult to create test patterns to verify an entire integrated circuit at the higher frequencies at which today's integrated circuits operate. Further, specialized testers are also required.

Detailed Description Text (9):
Following either of steps 218 or 222, and assuming that enough devices have been tested to form a statistically significant sample, the testing procedure continues to step 224 and the first and second ATE datalogs DATALOG1 and DATALOG2 are compared to ascertain the power supply voltage or range of voltages below which substantially all of the known good parts pass functional testing and above which substantially all of the "bad" parts fail functional testing. This voltage is referred to herein as the low voltage screen VDDS threshold. Next, in step 226, the low voltage screen VDDS threshold, is stored for use in a low voltage screening process of a production test program such as that described below in conjunction with FIG. 3. The test development procedure then ends in step 228.

CLAIMS:

1. A method for developing a low voltage screening process for testing integrated circuits on automated test equipment, the method comprising the steps of: providing an integrated circuit for testing;

applying a first power supply voltage to the integrated circuit;

executing test vectors of a functional test program the integrated circuit;

comparing the results of the functional test program with expected test results to determine if the integrated circuit passes the functional test; and, if so,

iteratively decrementing the first power supply voltage by a predetermined value and repeating the steps of executing test vectors and comparing the results until it is determined that the integrated circuit fails the functional test; and

storing a value representing the power supply voltage at which the integrated circuit first fails the functional test.

2. The method of claim 1, further comprising the steps of:

repeating each of the previous steps for additional integrated circuits; and

comparing the stored values to identify the lowest tested power supply voltage below which substantially all of the integrated circuits pass the functional test, the identified power supply voltage being useful for establishing a reduced voltage screening procedure for a production test program.

11. A method for testing integrated circuits on automated test equipment, the method incorporating a low voltage screening procedure, comprising the steps of:

providing an integrated circuit for testing;

applying a first power supply voltage to the integrated circuit, the first power supply voltage within the range of specified operating voltages for the integrated circuit;

executing test vectors of a production test program on the integrated circuit;

comparing the results of the production test program with expected test results to determine if the integrated circuit passes the production test program; and, if so,

reducing the first power supply voltage to a predetermined reduced voltage screening value;

executing test vectors of a screening test program on the integrated circuit; and

comparing the results of the screening test program with expected test results to determine if the integrated circuit passes the screening test program.

12. The method of claim 11, wherein the production test program and the screening test program are functional tests programs.

13. The method of claim 12, wherein the production test program and the screening test program are substantially the same.

20. The method of claim 19, wherein the screening test program is performed at a clock frequency less than the nominal operating frequency of the integrated circuit.

21. The method of claim 11, wherein the screening test program is performed at room temperature.

22. The method of claim 11, further comprising the step of marking the integrated circuit as a bad device if it fails the screening test program.

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L15: Entry 2 of 2 File: USPT May 6, 2003

DOCUMENT-IDENTIFIER: US 6560734 B1
TITLE: IC with addressable test port

Drawing Description Text (10):
FIGS. 9A, 9B, and 9C are block diagrams of an integrated circuit including a digital circuit and scan circuits in an intellectual property core and a test port, and FIGS. 9D, 9E, 9F, 9G, 9H and 9I are state diagrams describing testing procedures for the digital circuit.

Drawing Description Text (11):
FIG. 10A is a block diagram of an integrated circuit including a digital circuit and scan circuits in an intellectual property core and a test port, and FIGS. 10B, 10C, 10D and 10E are state diagrams describing testing procedures for the digital circuit.

Detailed Description Text (31):
Test port state machine 510 goes to or remains in the Reset Port state while RST is low, independent of the TPI input. When RST is taken high, the test port state machine is enabled to respond to TPI. The test port state machine remains in the Reset Port state while TPI is high, and transitions to the Enable Port state when TPI is low. The test port state machine remains in the Enable Port state while TPI is low, and transitions to the Scan Address Register state when TPI is high, to scan data through address register 401 from SI to SO.

Detailed Description Text (32):
The Scan Address State comprises three states, Capture, Shift, and Update, as indicated in FIG. 6B. The Capture state is used to capture status, pass/fail, match, and TPID data into the address register. The Shift state is used to shift out the captured data from the address register and shift in address and TE data to the address register. The TPID data shifted out primarily identifies the test port. However, the TPID data may contain additional information such as: the type of connected intellectual property (IP) core (DSP, CPU, I/O peripheral, memory, etc), the provider of the connected IP core (i.e. the company providing the IP), and IP core version. The pass/fail data shifted out indicates, as will be seen later, whether the core passed or failed a test. The status data shifted out indicates status conditions within the IC that may be useful to examine during test or functional IC modes. The match signal shifted out is used to test that the addressing circuitry of the test port is working correctly.

Detailed Description Text (35):
In the Input Port Address state, test port state machine 510 outputs control to input port 403 to cause the input port to store data present on IB, which is input via the ICs I/O as previously described in regard to FIGS. 2A. The data stored is an externally input address from an IC or wafer probe tester contacting the IC I/O at predetermined pads. With an 16-bit wide IB, one data input from IB provides addressing of up to 2.sup.16 -1 test ports, assuming the previously mentioned all zeros (initialization) address is not used for test port addressing. From the Input Port Address state, the test port state machine can transition to the Scan Address

Register state to re-scan the address register or to the Port Address Match state. The Port Address Match state is assumed to be the next state.

Detailed Description Text (42):
While an addressed test port state machine is in the Test Lock state, the enabled TPI controlled test operation state machine is unlocked to perform a test operation. When a TPI controlled test operation state machine has completed its test control operation, it also contains a lock state where it goes to and remains until an unlock sequence on TPI is received. When the unlock TPI sequence is received, the enabled TPI controlled test operation state machine outputs a reset signal to DFF 502 to set the lock signal low. Also, when the unlock TPI sequence is received, an addressed test port state machine is allowed to transition from the Test Lock state to either the Idle 1, Idle 2, or Scan Address Register state. Further, when the unlock TPI sequence is received, a non-addressed test port state machine is allowed to either remain in the Address Lock state, transition to the Idle 1 state, or transition to the Scan Address Register state. A TPI sequence that causes a transition from the Test Lock state to the Idle 2 state will cause the Address Lock state to be maintained. A TPI sequence that causes a transition from the Test Lock state to the Idle 1 state will also cause a transition from the Address Lock state to the Idle 1 state. A TPI sequence that causes a transition from the Test Lock state to the Scan Address Register state will also cause a transition from the Address Lock state to the Scan Address Register state.

Detailed Description Text (45):
When defining an escape TPI sequence, it is important to choose a sequence that is not used by any TPI controlled test operation state machine the when the TPI controlled test operation state machine is performing a test operation. Once the Sync state is entered, it will be maintained as long as TPI highs are received. The term Sync state is descriptive of the state's purpose in that it allows synchronizing the test port state machine and TPI controlled test operation state machines to a common state at the end of a test operation. When a TPI low is received a transition from the Sync state to the Next State 1 occurs. From Next State 1, a TPI low will cause a transition to Step 1 state, whereas a TPI high will cause a transition to Next State 2. From Next State 2, a TPI low will cause a transition to Idle 1, whereas a TPI high will cause a transition to Scan Address Register.

Detailed Description Text (47):
In both the Address Lock and Test Lock states, transitioning from the Sync state to Next State 2, via Next State 1, allows transitioning to either the Idle 1 or Scan Address Register states. Transitioning to Idle 1 allows addressing a new test port and performing the above described steps to allow a test operation state machine within the newly addressed test port to be enabled to perform a test operation on the core connected to the newly addressed test port. Transitioning to Scan Address Register state allows capturing and shifting the address registers of all test ports to load new data and to extract information from each test port, in particular pass/fail and status information. Also, transitioning to the Scan Address Register state is used to terminate testing and return the IC to functional mode by transitioning into the Reset State via the Exit Test Mode state.

Detailed Description Text (81):
In FIG. 9A, the test port is used to test a digital circuit 901 in connected core 900. Circuit 901 is designed with a test mode for configuring the circuit into a parallel scan path (PSP) arrangement. In this example the number of scan paths corresponds to the width of the test port IB and IOB busses, i.e. 16. Also, all scan paths have an equal number of scan cells. The mode (M) input from the test port is used to configure the core I/O and circuit 901 into the PSP test mode, as previously described in regard to FIG. 3.

Detailed Description Text (82):

In FIG. 3, the mode (M) input controlled multiplexers to connect inputs (I) from the test port to the test inputs (TI) of core circuit 901 and outputs (O) to the test port to test outputs (TO) from core circuit 901. An example of the parallel scan paths 1-16, is shown in FIG. 9B. An example of one of the scan paths coupled to combinational logic to be tested is shown in FIG. 9C. The scan path consist of a number of scan cells that test the combinational logic by inputting stimulus to and capturing response from the combinational logic during each scan cycle. Preferably, all the scan paths are designed with an equal number of scan cells, as this will expedite testing according to the present invention as described below.

Detailed Description Text (83):
To control the parallel scan path test configuration of FIG. 9A, a TPI controlled test operation state machine, as previously described in FIG. 5A, is provided within the test port.

Detailed Description Text (99):
During the autonomous test operation, counters 1 and 2 within input port 403 are controlled by control (C) output from the autonomous test operation state machine to load and count. Count data is written to the counters (see Input Test Mode state of FIG. 6A) prior to starting the autonomous test operation to provide the frequency of the count complete (CC1 and CC2) signals. The count complete signals determining how long the autonomous test operation state machine remains in the Generate & Shift data state (CC1) and Generate, Shift, & Compact Data state (CC1), and how many times to repeat the loop between the Generate, Shift, & Compact state and Capture Data state (CC2) In this example, counter 1 is loaded with a count equal to the scan cell length of the PSPs (all PSPs have equal scan cell lengths) and counter 2 is loaded with a count equal to the number of scan cycles required to input and output all stimulus and response patterns to the combinational logic being tested. Counter 1's count complete (CC1) signal indicates when all scan cells have been shifted in and out, and counter 2's count complete (CC2) signal indicates when all required stimulus and response patterns have been applied. In FIG. 9H, when a CC1=1 signal occurs, counter 1 is reload with the initial count data, except for when a CC2=1 signal occurs. When CC1=1 and CC2=1, the End Of Test state is entered.

Detailed Description Text (101):
In FIG. 10A, the test port is used to test another digital circuit 902 in connected core 900. Circuit 902 is designed with a test mode for configuring the circuit into a number of PSP groups. Each PSP group contains a number of scan paths corresponding to the width of IB and IOB busses of the test port, i.e. 16 bits. Also, the scan paths of each PSP group have the same number of scan cells, i.e. are equal in length.

Detailed Description Text (103):
Next, the test operation state machine enters the Shift Data state. In this state, the test operation state machine outputs control (C) to shift the data on the inputs (I) into the PSPs (via TI). This is a one shift operation state. This shift operation is used to input new stimulus data from the inputs (I) to the PSPs, and to output new response data from the PSPs to the outputs (O). After the shift operation, the test operation state machine re-enters the Read IOB Write IB state to read the response outputs (O) and input the next stimulus inputs (I). The test operation state machine will loop between the Read IOB Write IB state and Shift Data state a number of times to completely empty the PSPs of response and fill the PSPs with new stimulus. The number times this loop occurs is equal to the number of scan cells contained in the PSPs that need to be filled with stimulus and emptied of response

Detailed Description Text (169):
The following description assumes TPI controlled test operation state machines are used to test core 1-10. During the TPI controlled test operation, the test port

communicates with an external tester via CB, IB, and IOB. At the end of the TPI controlled test operation, the test port state machine 510 is unlocked. The unlocked test port state machine may transition to the Idle 2 state, the Idle 1 state, or the scan address states of FIG. 6A. Transitioning to the Idle 2 state permits inputting a new test mode into the currently addressed test port. Transitioning to the Idle 1 state permits addressing another test ports to perform a test on its connected core. Transitioning to scan address state permits scanning all test ports via SI and SO. Assuming the transition is to Idle 1, all test ports exit from Test and Address Lock states and go to Idle 1. Transitioning from the Idle 1 state to the Input Port Address state loads the new test port address. Transitioning from Input Port Address state to the Idle 2 state, via Port Address Match state, selects the newly addressed test port and places all non-addressed test ports into the Address Lock state. From the Idle 2 state, a transition to the Update Test Mode state, via the Input Test Mode state, selects a TPI controlled test operation state machine in the newly addressed test port and configures the connected core for testing. Transitioning from the Update Test Mode state to Test Lock state, unlocks and enables the TPI controlled test operation state machine and locks and disables the test port state machine. The core is then tested using the TPI controlled test operation state machine.

Detailed Description Text (179):
At the end of testing identical cores 6 and 7, the system test is complete. The address registers of all test ports are scanned to output their pass/fail information and to input data to place the system in functional mode. At the end of the scan operation, the tester evaluates the pass/fail information from each test port to see which core passed or failed a given test.

Detailed Description Text (192):
In FIG. 23B, a low cost IC tester is shown providing power (PWR), SI, IB, IOB, CB, SO, and ground (GND) contacts to the packaged ICs arranged on a test fixture 2301. Again, the tester is low cost because it only requires signals to power up the ICs, and communicate with the ICs serially via CB, SI, and SO, and in parallel via CB, IB, and IOB. The tester makes contact to each IC, via the signals above, using fixture 2301 which is designed to provide contacts between each IC and the tester. The tester can test all ICs on the fixture in parallel or in selected groups of parallel ICs on the fixture. The tests performed in parallel are as described on the individual system on chip in FIG. 20. The ability to test multiple ICs simultaneously using the compare test method of FIG. 20 reduces IC test time and thus IC manufacturing cost. After testing the ICs, the good ICs are tested at-speed on a conventional IC tester for final screening test. No ICs that fail the low cost test will get to the conventional at-speed tester, which again further reduces manufacturing cost by allowing only known good ICs to consume test time on the conventional IC tester.

Other Reference Publication (5):
Maunder, Colin, and Beenker, Frans, "Boundary-Scan: A Framework for Structured Design-for-Test," paper 30.1, International Test Conference 1987 Proceedings.

Other Reference Publication (7):
Whetsel, Lee, "A Standard Test Bus and Boundary Scan Architecture," pp. 48-59, Texas Instruments Technical Journal, Jul.-Aug. 1988, vol. 5, No. 4.